What is claimed is:

1. A semiconductor memory configured such that it can be connected with a first and second timing generator, the semiconductor memory comprising:

a first register configured to communicate with a memory array and the first timing generator, to retrieve and to hold first data from the memory array at a first timing;

a logic gate configured to communicate with the memory array and the first register, to receive the first data from the first register and second data from the memory array after the first timing, so as to compare the first and second data with each other, so that it can provide a comparison result indicating whether or not the first and second data agree with each other; and

a second register configured to communicate with the logic gate and the second timing generator, to retrieve and to hold the comparison result at a second timing.

2. The semiconductor memory of claim 1, further comprising a flip-flop circuit configured to communicate with the second register, and to hold a data disagreeing state if even one of the comparison results in the second register indicates that the first and second data disagree with each other.

3. A semiconductor memory configured such that it can be connected with a first and second timing generator, the semiconductor memory comprising:

a first register configured to communicate with a memory array and the first timing generator, to retrieve and to hold first data from the memory array at a first timing;

a second register configured to communicate with the memory array and the second timing generator, to retrieve and to hold second data from the

memory array at a second timing;

a delay circuit configured to communicate with the second timing generator, so as to delay the second timing, so that it can provide a third timing;

a logic gate configured to communicate with the first and second register, to receive the first data from the first register and the second data from the second register, so as to compare the received first and second data with each other, so that it can provide a comparison result indicating whether or not the first and second data agree with each other; and

a third register configured to communicate with the delay circuit and the logic gate, to retrieve and to hold the comparison result at the third timing.

4. The semiconductor memory of claim 3, further comprising a flip-flop circuit configured to communicate with the third register, and to hold a data disagreeing state once the comparison result in the third register indicates that the first and second data disagree with each other.

5. The semiconductor memory of claim 1, wherein:

the first timing is provided when output data is definite; and

the second timing is changed at intervals of clock cycles.

6. The semiconductor memory of claim 1, wherein:

the second timing is provided when output data is definite; and

the first timing is changed at intervals of clock cycles.

7. The semiconductor memory of claim 1, wherein:

the first timing is provided in response to rising or falling edge of a first strobe signal; and

the second timing is provided in response to falling or rising edge of a second strobe signal.

8. The semiconductor memory of claim 3, wherein:

the first timing is provided in response to rising or falling edge of a first strobe signal; and

the second timing is provided in response to falling or rising edge of a second strobe signal.

9. The semiconductor memory of claim 3, wherein:

the first timing is provided in response to a rising edge of a first strobe signal; and

the second timing is provided in response to a falling edge of the first strobe signal.

10. The semiconductor memory of claim 1, wherein the first register receives a clock signal instead of the first data.

11. The semiconductor memory of claim 2, wherein an output of the flip-flop circuit is supplied to a shift register of a boundary scan circuit.